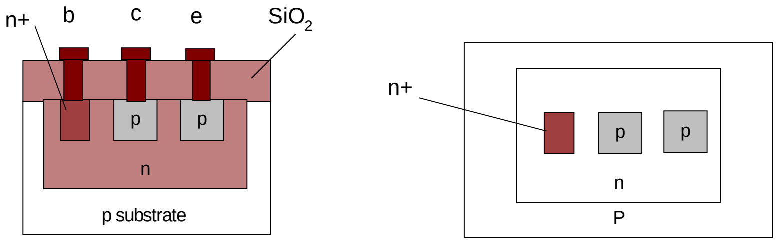
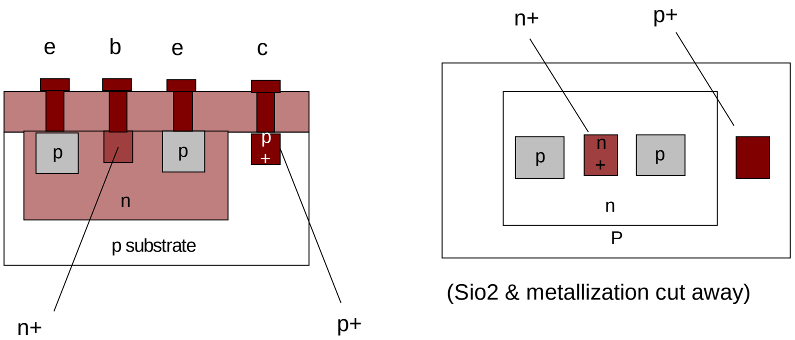
IC Fabrication : Transistor types



(Sio2 & metallization cut away)

Lateral PNP transistor



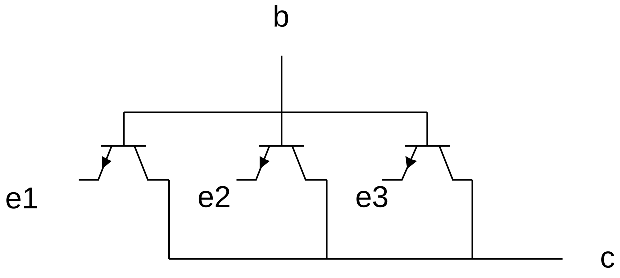
(Sio2 & metallization cut away)

Vertical PNP transistor

Lateral PNP has smaller Beta as injection efficiency of P type emitter < n+ in NPN. Base area is larger and some minority holes migrateinto substrate. Hence low collector current. NPN used only with fixed negative collector. i.e. emitter follower.

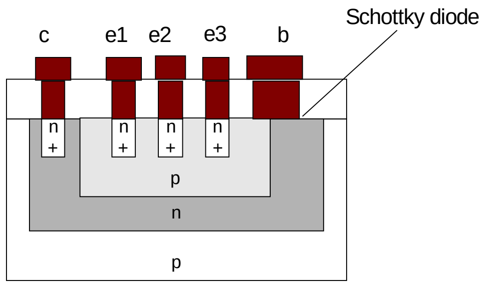
Multi-Emitter:

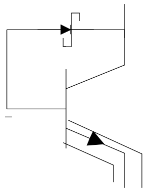
TTL uses multiple transistors sharing common base and collector connections. This is fabricated using a single collector diffusion, single base diffusion and multiple regions having emitter diffusions, saving space.



Schottky Transistor:

Uses metal-n type junction as a Schottky diode.
This acts as a clamp between C & B limiting forward bias voltage to 0.4 volts and preventing saturation. Since excess carriers due to saturation are absent, less time is required to remove carriers while going from ON to OFF state. Used in Switching transistors.

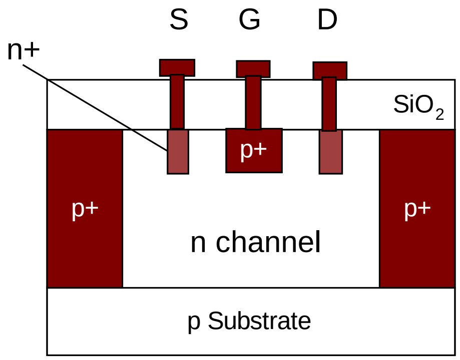




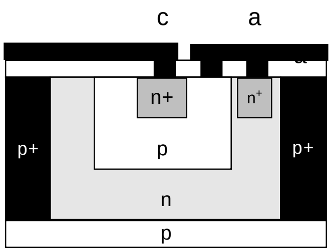
Super BETA transistors:

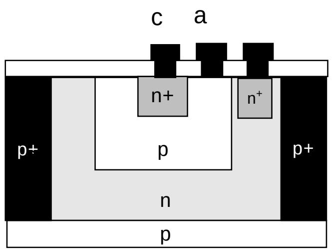
Normal Beta is about 150. If Emitter is made to penetrate deeper into p type base higher BETA obtained because of narrower base layer. E-B breakdown voltage however reduces. Hence suitable for low voltage applications

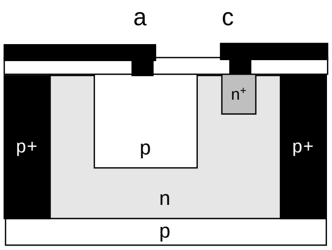
JFET:



Diodes:







a) Using E-B diode with collector short-cicuited to base.
b) E-B diode with collector open,

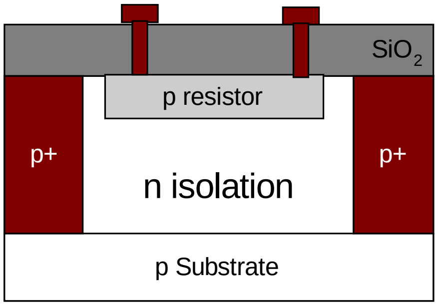
Both above versions are popular for applications with low voltages, as E-B diode breakdown is low Common anode arrays in a single isolation area are possible using multi-emitter diffusion

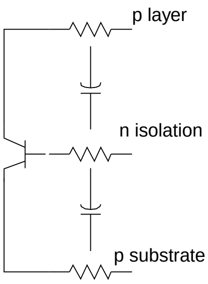
c) C-B diode with E open or missing. These have higher C-B voltage breakdown rating, suitable for common cathode diode arrays within a single isolation island. Common anode arrays require separate isolation, anodes are then connected by metallization.

Resistors:

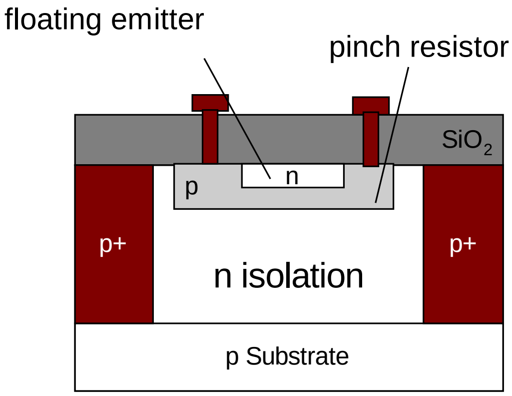
a) Using bulk resistivity of p type base: sheet resistance inversely proportional to thickness: Base diffusion typically 200 ohms/um^2 , R = RsL/W. Different values by choosing L and W. The n- epitaxial layer isolates resistance from other components. Precision not possible, and hence design uses R ratios rather than absolute values.

Width > 5um practical values 20 ohm - 30 kohm





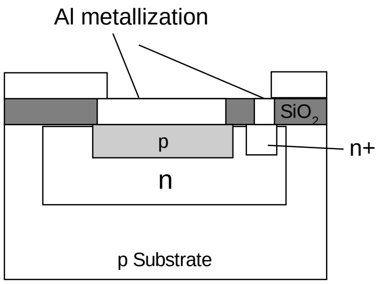
b) Ion implanted resistance: have better tolerance specs.
c) Epitaxial resistances: have higher resistance (about 6 times)
d) Pinch resistance obtained by adding n diffusion to restrict conducting area. Current cannot flow through the n-p contact in reverse direction. Higher resistance using an epitaxial pinch resistor. Reverse breakdown voltage b-e apply to pinch resistors.

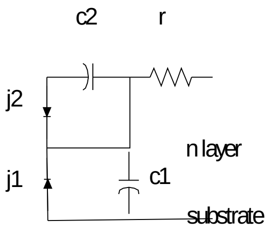


e) MOS and polysilicon deposition have higher resistance.
f) Thin film : vapor deposited film of NiCr on SiO layer with mask etching used. Covered by insulating layer (20 Ohm - 50 Kohm) Precise values possible with laser trimming.

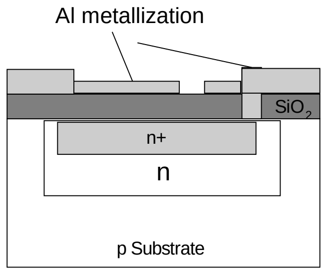
Capacitors:

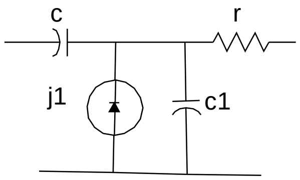
a)Junction capacitor formed by the reverse biased epitaxial n and upper p layer junction. Other Jn. gives a parasitic capacitance. Minimised by making substrate most negative.



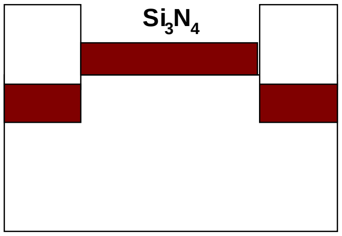


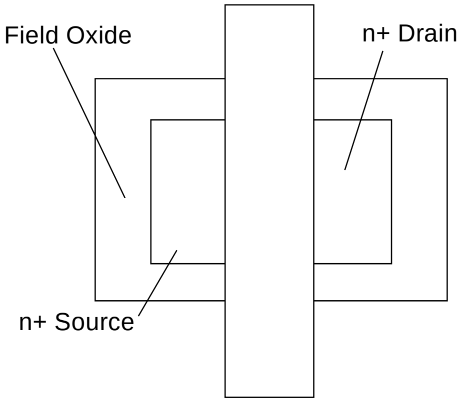
b)MOS/Thin Film capacitor: Parallel plate with SiO as dielectric, Al top plate and n+ region is the bottom plate.

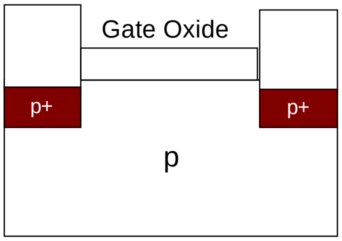

Al metallization
SiO$_2$
n+
n
p Substrate

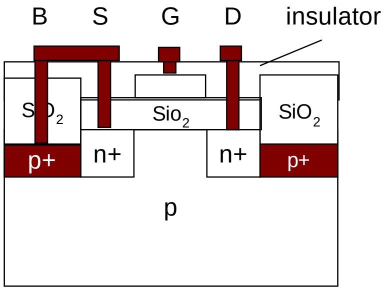

c
r
j1
c1

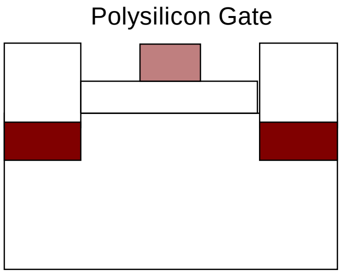
MOSFETS:

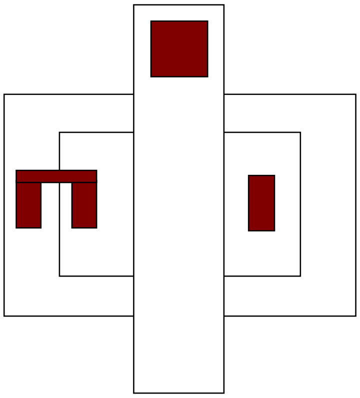

Si$_3$N$_4$


Field Oxide
n+ Drain
n+ Source


Gate Oxide
p+
p+
p


B
S
G
D
insulator
SiO$_2$
Sio$_2$
SiO$_2$
p+
n+
n+
p+
p


Polysilicon Gate



Diffusion:

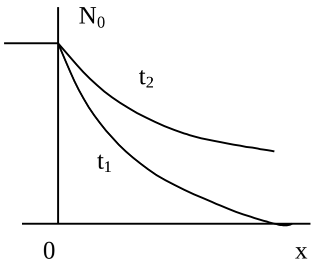
Diffusion Equation:

Governs the diffusion of atoms in the substrate, $dN/dt = D\,(d^2N/dx^2)$ where N is th concentration in atoms /unit volume as a function of the distance x and time t, D is the diffusion constant. In area/unit time
The number of atoms diffusible should be less than the solid solubility of the atoms in the material, which is defined as the maximum concentration which can be dissolved in the substrate. Solid solubility varies with materials and temperature and is available as graphical data.
Diffusion coefficients are also a function of temperature, and are doubled for a few degrees rise in temperature. This data is also availble, and a chosen value of D is maintained by accurate control of process temperature.
A volume of Gas with concentration N_0 of say n- type impurity, i.e. phosphorus will produce a distribution obtained by solving diffusion equation with boundary condition that N_0 at surface is constant, and N(x) = 0 at t = 0. The solution is

$$N(x,t) = N_0\left(1-erf\,\frac{x}{2\sqrt{Dt}}\right) = N_0 erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

$$erf(y) = \frac{2}{\sqrt{\pi}}\int_0^y e^{-\lambda^2}\,d\lambda$$

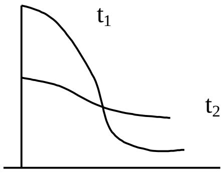
and erfc (y) = 1 – erf(y)



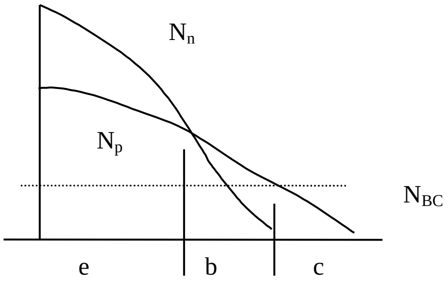
If a specific number Q of atoms per unit area are deposited and material is heated, boundary condition becomes

$\int N(x)\,dx = Q$ and N(x) = 0 at t = 0

then $N(x,t) = \dfrac{Q}{\sqrt{\pi Dt}}\,e^{-x^2/4Dt}$ which is a Gaussian distribution.



Typical impurity profile is shown below:



A uniformly doped n type layer of.5 ohm/cm resitivity is subjected to Boron diffusion with boron concentraion 5×10^{18} atoms/cm^3 A junction is desired at 2.7 um after a 2 hr process. What temperature?
Background n = ρ /mobility×q= $1/(0.5 \times 1300\times(1.6\times10^{-19})) = 0.96\times10^{14}$ cm^{-3}
Junction is formed when N = n
Thus erfc (y) = $n/N_0 = 1.98\times10^{-2}$ = 2.2
Then $2.2 = 2.7\times10^{-4}/(2\times\sqrt{}\,(D\times2\times3600))$
Thus $D = 5.2\times10^{-12}$
This value is obtained at 1130 degrees from curves of D vs. temp.