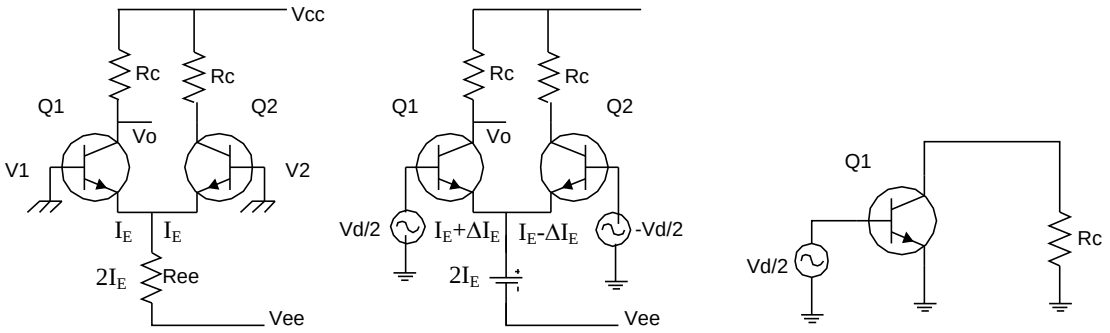
The differential amplifier

The emitter coupled differential amplifier output is $V_o = A_d V_d + A_c V_C$
Where $V_d = V_1 - V_2$ and $V_C = (V_1 + V_2) / 2$
In the ideal differential amplifier A_c should be zero and A_d should be as high as possible,
To find A_d , we apply a purely differential signal V_d to the amplifier, with $V_C = 0$
Then $Vo = A_d V_d$, and we can find A_d .
To find A_c , we apply purely common mode signal $V_1 = V_2 = V_C$ so that $Vo = A_c V_C$.
From this we an find A_c .
In the general case, after finding A_d and A_c we can calculate Vo for given inputs.

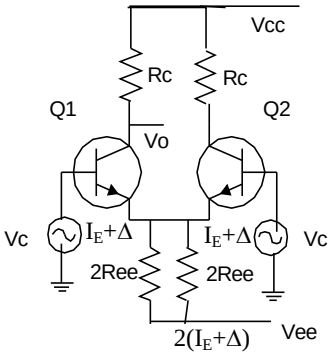
EMITTER COUPLED DIFFERENTIAL AMPLIFIER

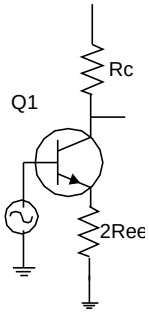
Gain A_d:



The differential mode gain is obtained by applying a differential signal. In quiescent state, both inputs are 0 and the emitters carry equal currents I_E . The current in R_{EE} is $2I_E$.
When differential signal is applied, Q1 current increase to $I_E + \Delta I_E$ and Q2 current decreases to $I_E - \Delta I_E$.
The current in R_{EE} remains $2I_E$.
Thus voltage across R_{EE} does not change from quiescent value, even when signal is present.
The voltage V_E therefore remains constant, and is equivalent to a DC voltage source equal to $2I_E R_{EE}$ were connected in place of R_{EE} .
For signal analysis equivalent circuit, a dc source is equivalent to a short circuit for the signal.
Thus for the signal $V_d/2$ the emitter of Q1 and Q2 are effectively grounded.
The circuit can therefore be bisected along the central axis of symmetry, without changing any signal voltages or currents, and the half circuit is a CE amplifier circuit.
The gain therefore is $Vo /(V_d/2) = - h_{fe} R_C / h_{ie}$ and the input resistance of each half circuit is h_{ie} .
Thus $Vo /V_d = A_d = - h_{fe} R_C /2 h_{ie}$ and differential input resistance is $h_{ie} + h_{ie} = 2 h_{ie}$ across the two input terminals

COMMON MODE GAIN:
Initially consider Quiescent state. The current in R_{EE} is $2I_E$. Now give a pure common signal V_C to both inputs. The current in both transistors increases to $I_E + \Delta$ each. Current in R_{EE} is now
$2(I_E + \Delta)$.
Now replace R_{EE} with two resistors , each of $2R_{EE}$ value in parallel. This will not change the circuit in any way.
The current in each parallel resistor of $2R_{EE}$ is $2(I_E + \Delta)/2 = (I_E + \Delta)$.
Thus ALL the current coming from each emitter $(I_E + \Delta)$ goes into the nearest $2R_{EE}$ resistance.
There is no current in the link joining the tops of the two $2R_{EE}$ resistors., so we can safely open that link without affecting behaviour of the circuit.
The original circuit can now be cut along the axis of symmetry to form two identical half circuits.
Each half circuit is a CE with R_E where $R_E = 2R_{EE}$
Hence gain $Vo/V_C = A_c = -h_{fe} R_C /(h_{ie} + (I + h_{fe}) 2R_{EE}) \cong -R_C /2R_{EE}$ for large h_{fe} and normal h_{ie}
The common mode input resistance is $h_{ie} + (I + h_{fe}) 2R_{EE}$





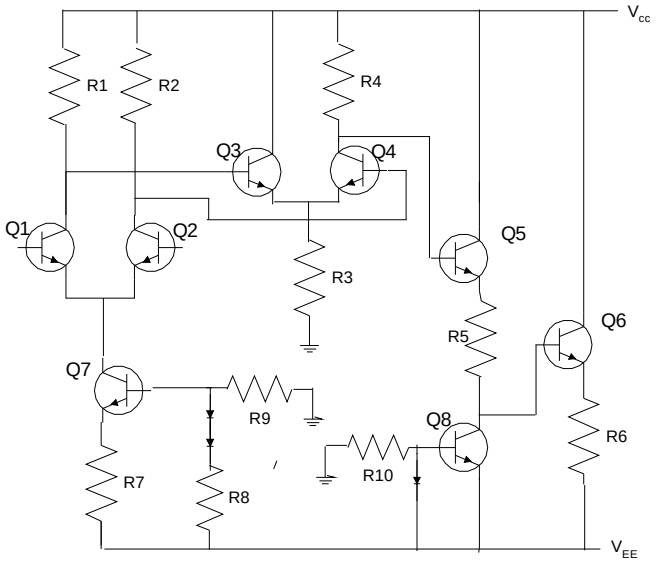
CMRR improvement:

CMRR can be improved by

1. Increasing R_{EE} . This is possible only up to a certain limit decided by the power supply voltage and transistor bias current. The Integrated circuit area problem and the theoretical limitations also exist as in CC case.
2. Replacing R_{EE} by a current source.
3. Using active load (current sources) as R_C for getting high differential gain
4. Using cascaded differential amplifiers. However, direct coupling means that V_c of the first stage will be V_B of the next stage. That in turn means that V_C of the next stage will be even higher, with value approaching the V_{cc} value. The next stage transistor will then get cut-off even with a small input, giving a relatively smaller swing in output voltage. For this reason it is not practical to cascade more than two stages.

Analysis and design of MC1530:

The conditions for the analysis and design are



1. All transistors have h_{fe} = 100, and use $V_{cc} = -V_{EE}$ = 6V,
2. Transistors Q1 to Q4 have I_C = 0.5 ma, Q5 has I_C =1.56 ma and Q6 has I_C = 5 ma
3. All current sources are current mirrors with equal current in each branch.
4. First stage is designed for maximum differential gain within a limited range of input voltage, and very high CMRR by using a current source as R_{EE} . The range of input voltage is decided by ensuring that Q7 does not saturate.
5. The second stage is designed for maximum A_d with A_c =1. This can be done as the first stage takes care of the CMRR.
6. The voltage shifter and output stages are designed to get 0 output in quiescent (no signal) case.

Calculation of current source resistances:

R7:

The current source Q7 has to be active for the amplifier to work. Then $V_{CE7} \cong V_{EE}/2 = 3V$

The inputs are at ground, Hence the top of R7 is at $0 - V_{BE1} - V_{CE\,7}$ and bottom is at V_{EE} -

so voltage across R7 = $(0 - 0.7 - 3.0) - (-6) = 2.3V$

current through R7 = $I_{E1} + I_{E2} \cong I_{C1} + I_{C2} = 0.5 + 0.5 = 1$ mA.

Hence R7 = 2.3 K, but we choose the nearest standard value 2.2K

Thus R7 = 2.2K

R8:
With R7 = 2.2K voltage $V_{B7} = -6 + (2.2K \times 1ma) + V_{BE7} = -6 + 2.2 + 0.7 = -3.1V$
The drop in the two diodes is $0.7 \times 2 = 1.4V$
Then top of R8 is at $V_{B7} - 2V_D = -3.1 - 1.4 = -4.5$ V
Bottom is at −6 V.
Then $V_{R8} = -4.5-(-6) = 1.5V$, $I_{R8} = 1$ mA (current mirror action)
Hence R8 = 1.5K

R9:
V_{B7} is −3.1V, hence across R9 voltage is 3.1V. current is 1 mA, hence R9 = 3.1K

Calculation of differential stage

R1 and R2 :
The Q7 transistor being a current source has to remain active for the amplifier to operate.
Base voltage of Q7 is −3.1V, and under quiescent conditions, V_{C7} is $= -V_{BE1} = -0.7V$.
When a negative signal is given to base of Q1, say −V, then the emitter voltage is −V−0.7
And hence V_{C7} is −V−0.7. If this voltage is lower than V_{B7} by 0.5 V then Q7 will saturate.
Thus Q7 saturates at $V_{C7} = -3.1 - 0.5 = -3.6V$.
Corresponding V_{B1} is $-3.6 + 0.7 = -2.9$ V
Thus input cannot be made more negative than −2.9 V or Q7 will saturate.
For safety we limit input to −2.7V
Then in positive half cycle, max $V_{B1} = 2.7V$
Now for maximum differential gain R_C should be maximum. As R_C is made large, drop across it increases and V_{C1} becomes lower. If V_{C1} is less than V_{B1} by 0.5 then transistor Q1 will saturate.
So minimum allowable $V_{C1} = 2.7 - 0.5 = 2.2$ V. Below this Q1 will saturate.
Then drop across R1 = 6 −2.2V = 3.8V
Current through R1 = 0.5mA hence R1 = R2 = 3.8/0.5 = 7.6K

Gain stage resistance:

R3:
With R1 = 7,6K , $V_{C1} = V_{cc} - I_{C1} R1 = 6 - 7.6 \times 0.5 = 2.2V$
Then $V_{B3} = V_{C1}$ and $V_{E3} = 2.2 - 0.7 = 1.5V$
Then voltage across R3 = 1.5V and $I_{R3} = I_{E3} + I_{E4} = 0.5 + 0.5 = 1$ mA
So R3 = 1.5K

R4:
With R3 = 1.5K , to get max differential gain R_C should be largest.
Increasing R_C increase |common mode gain| as well, and this has to be kept ≤ 1
Thus max value of R_C we can use will make $|A_c| = 1 = R_C/2R_{EE}$
Then $R_C = 2R_{EE} = 2 \times 1.5K = 3K$
Therefore R4 = 3K

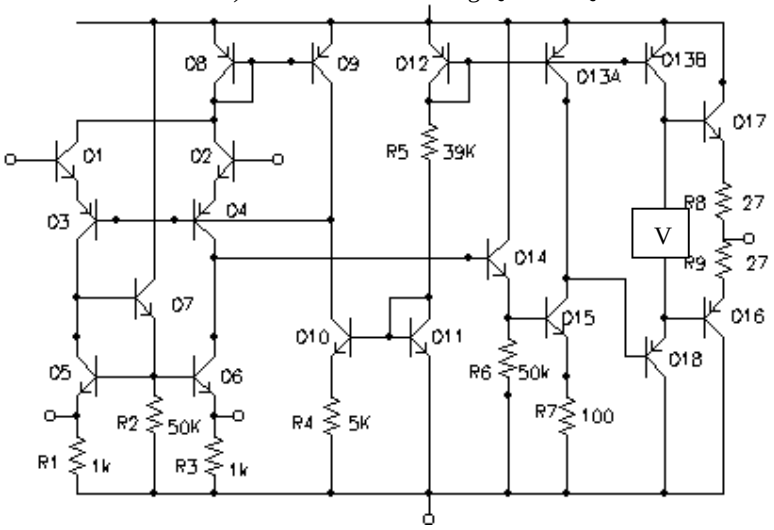
Voltage shifter and output stages:

R5:
With R4 = 3K, $V_{C4} = 6 - 3 \times 0.5 = 4.5V$.
So $V_{E5} = 4.5 - 0.7 = 3.8V$
Now for 0 input output voltage i.e $V_{E6} = 0$.
Then $V_{B6} = 0.7V$
The voltage across R5 = 3.8 − 0.7 = 3.1 V, and current =1,56 mA , giving
R5 = 2K
R10:
Voltage across R10 is $V_{EE} + V_d = -6 + 0.7 = -5.3V$, and current = 1.56mA
Then R10 = 5.3/1.56 = 3.1K
R6:
Vo = 0 in quiescent state, so across R6 we have 6V. current is 5 mA,
so R6 = 1.2K

741 OPERATIONAL AMPLIFIER

The 741 Op Amplifier has four stages:

1. Input differential stage: Q1and Q2 are CC input transistors with high R_{in}. They are cascaded with Q3 and Q4 which are CB differential voltage amplifier, their low i/p impedance matching with low output impedance of the previous CC stage. Q5, Q6 and Q7 are the current sources which act as active load for Q3 and Q4, Q8 acts as the common resistor (like R_{EE} in the standard circuit). The branch containing Q12 and Q11 decides bias current. If this branch



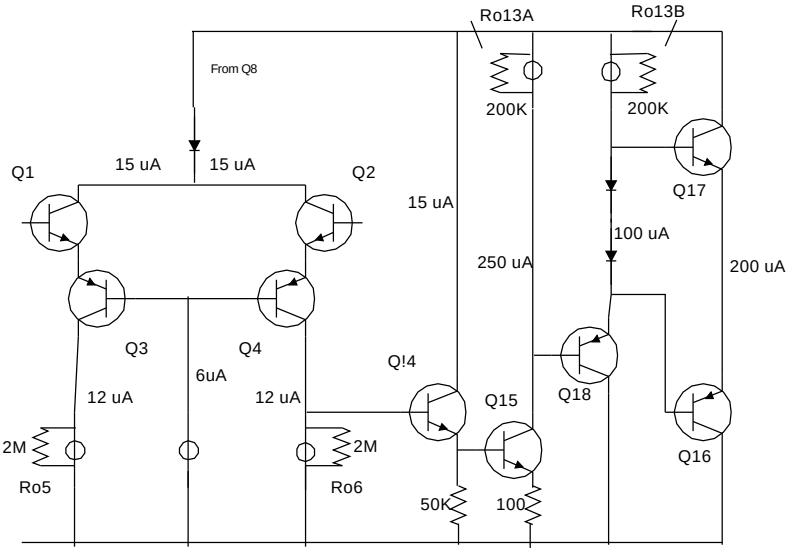
has current I_4, then the branch with Q9, Q10 has a much smaller current I_3 because Q10-Q11 are widlar source. I_0 in Q8 in the differential amplifier = I_3 as Q8 and Q9 are current mirror. These current mirrors are used to provide the bias currents.

2. The gain stage has buffer CC Q14 and amplifying CE with R_E Q15. The Q15 load is active load given by current mirror transistor Q13A, and the output is buffered by Q18 which passes it on to the output stage.
3. The Q13B and the block labelled V is the voltage shifter for ensuring the the two output transistors are ON under 0 input conditions, Then $V_o = 0$ as it is the electrical centre of the output branch . Block "v" is a V_{BE} multiplier .
4. Output is complimentary pair of transistors. Under 0 input both are ON when +ve i/p is given at Q18 base, Q17 conducts and Q18 cuts off, delivering current into load. During negative input Q18 conducts and Q17 cuts-off thus current is taken from load.
5. Under 0 input condition $I_2 = I_1$ and $I = I_1$ (current mirror) so $I_d = I_2 - I = 0$, hence no input to the next stage, and output stays 0V
6. When positive i/p is given to Q1, current I_1 increases, and I_2 decreases. Hence $I_2 - I = I_d$ is drawn from the next stage.
7. When negative i/p is given to Q1, current I_1 decreases, and I_2 increases. Hence $I_2 - I = I_d$ is delivered to the next stage.
8. The amplifier first stage is thus a trans-conductance amplifier.

Analysis of differential gain of 741

The currents in the various current sources are shown in the figure, which gives the important sub-circuits of the 741. All Transistors have $h_{fe} = 200$ and Q3 and Q4 have $h_{fe} = 4$.

The input stage transistorsQ2 and Q4 with their load Ro6 and R_i14 are shown in the second figure. Output resistance of Q6 and input resistance of Q14. Appear as parallel load to Q4 collector.



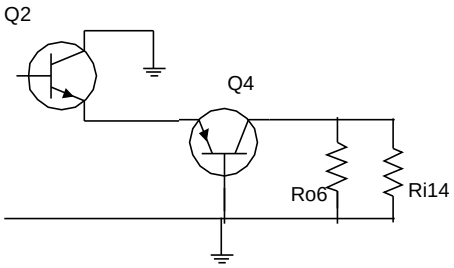
R_{id} calculation:

Here $R_{id} = 2R_{i2} = h_{ie2} + (1+h_{fe2})R_{i4}$ and $R_{i4} = h_{ie4}/(h_{fe4}+1)$

$$hence \quad R_{id} = \left(\frac{h_{fe2}V_T}{I_{C2}} + \frac{1+h_{fe2}}{1+h_{fe4}} \frac{h_{fe4}V_T}{I_{C4}} \right)$$

here I_{c2} = 15 uA and I_{C4} = 12 uA
giving $\underline{R_{id} = 1.38\ M\Omega}$

1st stage gain:

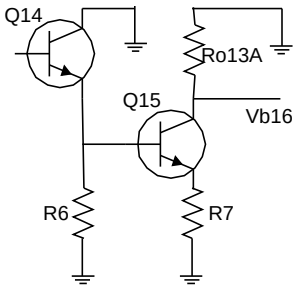


$R_{L4} = Ro_6 \parallel R_{i14}$
And output of first stage = $V_{b14} = i_{c4} \times R_{L4}$
Now $i_{c4} = h_{fe4} / (1+h_{fe4})i_{e4}$
With $i_{e4} = (1+h_{fe2})i_{b2} = (1+h_{fe2})v_{id}/2r_{i2}$

Then, $$\frac{v_{b14}}{v_{id}} = \frac{h_{fe4}}{1+h_{fe4}} \frac{1+h_{fe2}}{r_{id}} R_{L4}$$

Now $h_{ie14} = h_{fe14}V_T / i_{c14}$ = 350K. Similarly h_{fe15} = 21K
Then $R_{i15} = h_{ie15} + (1+h_{fe15})R_7$ = 41K
Then $R_{i14} = h_{ie14} + (1+h_{fe14})(R_6 \parallel Ri_{15})$
Giving R_{i14} = 4.88 M
Using values of R_{i14} and R_{o6}, R_{L4} = 1.42M, giving
First stage gain = V_{b14}/V_{id} = 166

Second stage gain



If we assume that R6 was not present then
$i_{b15} = (h_{fe}+1)i_{b14}$
Then $i_{C15} = h_{fe15}h_{fe14} I_{b14}$
With R_6, there is a loss of current and the new gain is $\beta = h_{fe15}h_{fe14} (R_6/(R_6 + R_{i15}))$
Neglecting drop in Q18
$v_{b16}/v_{b14} = -\beta (R_{o13}/R_{i14})$
h_{fe14} and h_{fe15} can be calculated and are 350K and 21K.
then $R_{i15} = h_{ie15} + (1+h_{fe15})R7$ = 41K, and $R_{i14} = h_{ie14} + (1+h_{fe14})(R_6 \parallel Ri_{15})$ = 4.88M
$\beta = 200 \times 200 \times (50/(50+41))$ = 22000
$\underline{\text{Second stage gain} = v_{b16}/v_{b14} = -22000\ (0.2/4.88) = -902}$

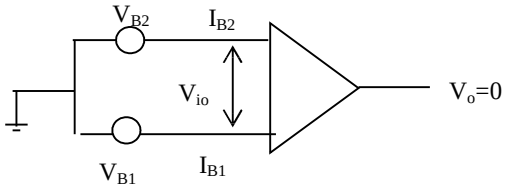
thus $\underline{A_d = 166 \times -902 = -150000}$

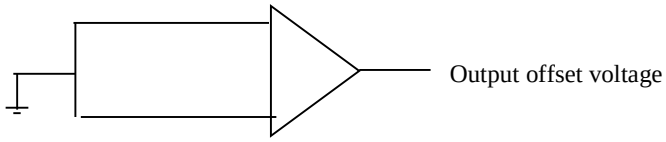
OUTPUT RESITANCE:

For small signals Q16 and Q17 are in parallel as their bases are connected.
Then $R_0 = [(R_{o18} \parallel R_{o13A}) + (h_{ie17} + h_{ie16})] / (h_{fe17}+1)$
And $R_{o18} = (R_{o13B} + h_{ie18}) / (h_{fe18} + 1)$
Now h_{ie17} = 26K (By calculation)
h_{ie18} = 26K and h_{ie18} = 52K giving R_{o18} = 1.25K
Then $R_{o18} \parallel R_{o13A}$ and
R_o = 1.25 + (26||26) / 201 =71 Ohm
Thus each transistor has o/p resistance 142 Ohms.
Now each transistor is in series with 27 Ohm, so final output resistance is
(142+27)||(142+27) = 83 Ohms

SPECIFICATION PARAMETERS OF OP-AMPS

Input Bias Current (I_B) : average current entering i/p terminals when amplifier is balanced i.e. v_o = 0 Typical 100nA
Input Offset Current (I_{io}): difference between currents entering input terminals when v_o=0. Typical:10 nA





Input Offset Current Drift: ratio of change in I_{io} upon change in absolute temperature. Typical 0.1nA/degree C
Input Offset Voltage (V_{io}): Voltage at the input terminals to balance the amplifier. Typical 1mV
Input Offset Voltage Drift: Ratio of change in input offset voltage to the change in temperature. Typical 1uV/degree C
Output Offset Voltage: Output voltage when inputs are grounded.
Power Supply Rejection Ratio: Ratio of change in input offset voltage to the change in any one of the power supply voltages. Typical 20 uV/V
Slew Rate: Time rate of change of the closed loop amplifier output voltage under large signal conditions. Typical 1V/uS
Open Loop Gain: typical 50000
CMRR: Typical 100dB

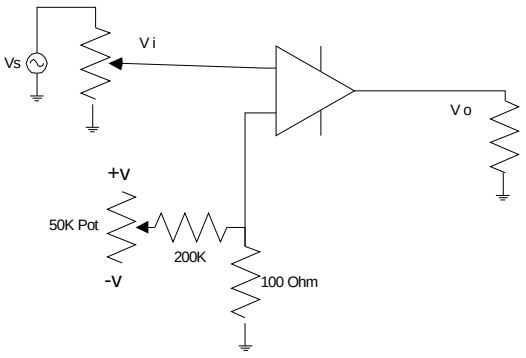
Measurement:

A_v

Measure output signal voltage without R_L , ensuring output voltage is not more than 30% of rating. Find A_v

Output Resistance:

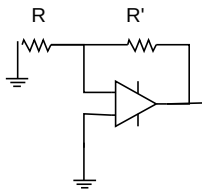
Attach R_L and measure gain.
Then $A_V = R_L/(R_L + R_o)$ A_v and so $R_o = ((A_v/A_V)-1)R_L$



R_{id}:

Insert two equal resistors in series with the two input terminals measure output.
Then new output $V_o' = [R_{id} / (R_{id} + 2R)]\ V_o$ where Vo is the output without the two resistances.
Then $R_{id} = 2R [V_o' /(V_o – V_o')]$

V_{io}:

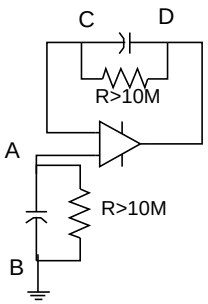


Connect circuit as shown. Then v_{io} exists between input terminals
From the circuit $V_o = [(R+ R')/R]\ V_{io}$
Take R = 100 Ohm and R' = 100K for easy measurement.

I_{io} and I_B:

Use large resistance > 10M as shown, with noise bypassing capacitors. (0.01uF)

Connect A and B short-circuiting the lower resistance.
then measured output is $V_o = I_{B2}R.$, from which I_{B2} is obtained
If we short-circuit C and D and measure output,
$V_o = -I_{B1}R.$ which gives I_{B1}.Thus I_{B1} and I_{B2} can be found.
From this $I_B = (I_{B1} + I_{B2})/2$ and $I_{io} = I_{B1} - I_{B2}$



The capacitors are used to bypass effects of noise voltage which is generated by random flows of electrons in the resistance. At the high resistance used, this voltage is significant.

CMRR:

Using circuit shown, with R =R1 = 100 Ohms and R' = R1' = 100K we can calculate CMRR as follows:

Voltage across $R = V_i - [V_s R_1/(R_1+R_1')]$
Across $R' = V_o - Vi - [V_s R_1'/(R_1+R_1')]$
Assuming equal currents in R and R' (neglecting input bias current) and noting that $R = R_1$ and $R' = R_1'$ and solving,
$V_i = (R/(R+R'))V_o$
$V_c = V_s [R_1'/(R_1 + R_1')] = V_s [R'/(R + R')]$
Also $V_o = A_d V_d + A_c V_c = [(A_d R V_o)/(R+R')] + [(A_c R' V_s)/(R+R')]$
Thus $V_o[1 - (A_d R/(R+R'))] = (A_c R' V_s)/(R+R')$
By choosing R and R' such that $A_d R/(R+R') >> 1$
$-V_o A_d R/(R+R') = A_c R' V_s/(R+R')$
and so
$|A_d/A_c| = (R'/R)(V_s/V_o)$ which is the CMRR.